SY8286A

High Efficiency Fast Response 6A, 23V Input Synchronous Step Down Regulator

General Description

The SY8286A develops a high efficiency synchronous step-down DC/DC regulator capable of delivering 6A current. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

The SY8286A operates over a wide input voltage range from 4V to 23V. The DC/DC regulator adopts the instant PWM architecture to achieve fast transient responses for high step down applications and high efficiency at light loads. The device provides various protection features for reliable operation. In addition, it operates at pseudo-constant frequency of 600kHz to minimize the size of inductor and capacitor.

Ordering Information

SY8286 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8286ARAC	QFN3×3-20	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 38/19 mΩ
- Wide Input Voltage Range: 4-23V
- Instant PWM Architecture to Achieve Fast Transient Responses
- Internal 1.3ms Soft-start Limits the Inrush Current
- Pseudo-constant Frequency: 600kHz
- 6A Output Current Capability
- ±1% Internal Reference Voltage
- PFM/PWM Selectable Light Load Operation Mode
- Optional Bypass Input
- Power Good Indicator
- Output Discharge Function
- Output Current Limit Protection
- Hiccup Mode Output Short Circuit Protection
- Output Over Voltage Protection
- Input UVLO
- Over Temperature Protection with Auto Recovery
- RoHS Compliant and Halogen Free
- Compact Package: QFN3×3-20

Applications

- LCD-TV/Net-TV/3DTV
- Set Top Box
- Notebook
- High Power AP

Typical Applications

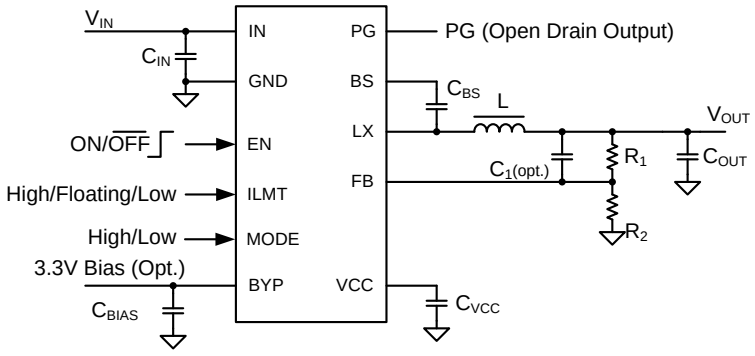


Figure1. Schematic Diagram

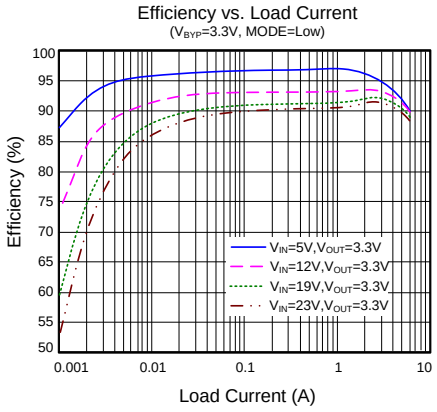
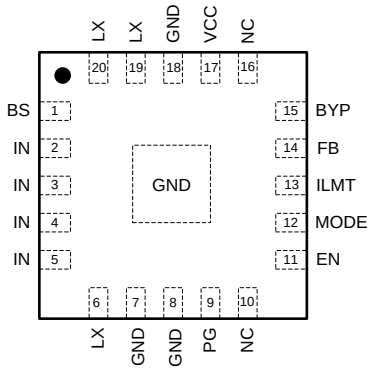


Figure2. Efficiency vs. Load Current

Pinout (top view)



(QFN3×3-20)

Top Mark: AWR*xyz*, (Device code: AWR, ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.
IN	2,3,4,5	Input pin. Decouple this pin to the GND pin with at least a 10μF ceramic capacitor.
LX	6,19,20	Inductor pin. Connect this pin to the switching node of the inductor.
GND	7,8,18,EP	Ground pin.
PG	9	Power good Indicator. Open-drain output when the output voltage is within 90% to 120% of regulation point.
NC	10, 16	Not connected
EN	11	Enable pin. Pull this pin high to turn on the IC. Do not leave this pin floating.
MODE	12	Operating mode selection under light load. Pull this pin low for PFM operating, and pull this pin high for PWM operation. Do not leave this pin floating.
ILMT	13	Output current limit threshold selection.
FB	14	Output feedback pin. Connected to the center point of the resistor divider.
BYP	15	External 3.3V bypass power supply input. Decouple this pin to the GND with a 1μF ceramic capacitor. Leave this pin floating if it is not used.
VCC	17	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to the GND with a 2.2μF ceramic capacitor.

Block Diagram

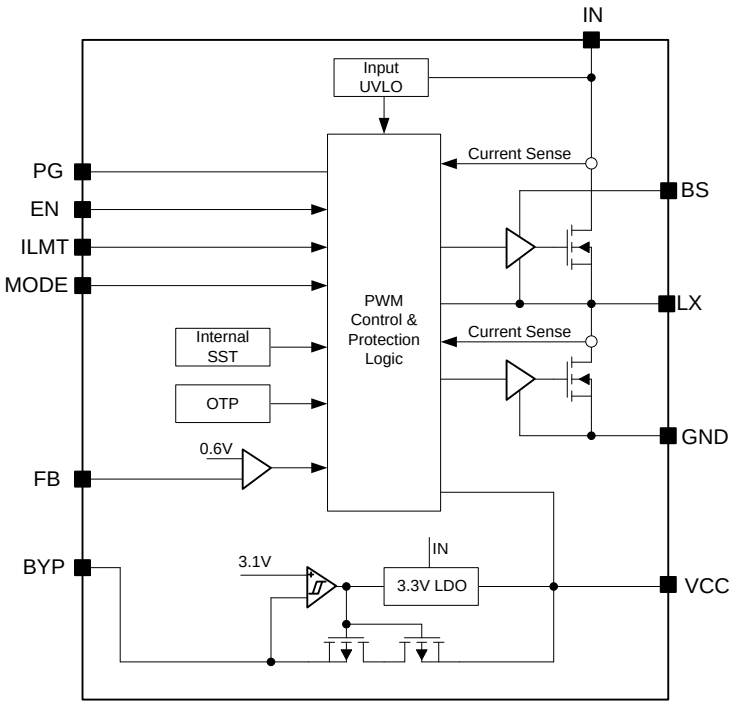


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN ---------- 25V
BS-LX ---------- 4V
EN, ILMT, MODE, PG, LX ---------- 25V
VCC, FB ---------- 4V
BYP ---------- 6V
Power Dissipation,
P_D @ T_A = 25℃ QFN3×3-20 ---------- 3.3W
Package Thermal Resistance (Note 2)
θ_{JA}, QFN3×3-20 ---------- 30℃/W
θ_{JC}, QFN3×3-20 ---------- 4.5℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
Dynamic LX voltage in 10ns duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4V to 23V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(V_{IN} = 12V, T_A = 25℃ unless otherwise specified)

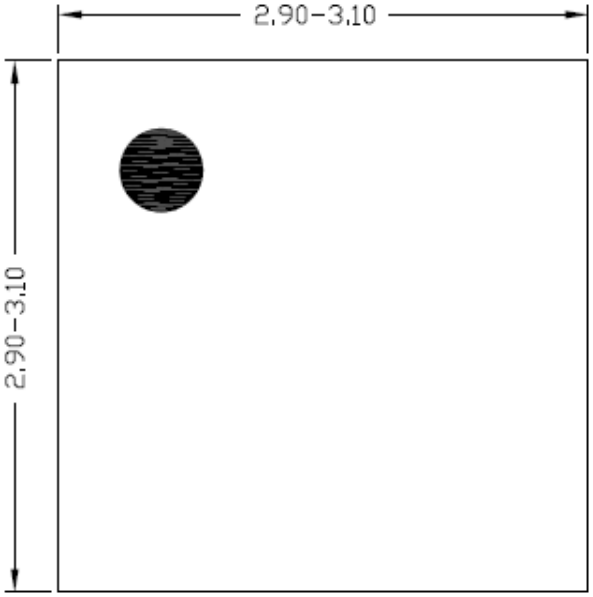
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		23	V
Input UVLO Threshold	V_{UVLO}	V_{IN} rising			3.9	V
UVLO Hysteresis	V_{HYS}			0.1		V
Quiescent Current	I_Q	I_{OUT}=0, V_{OUT}=V_{SET}×105%		120	145	μA
Shutdown Current	I_{SHDN}	EN=0,		6	10	μA
Feedback Reference Voltage	V_{REF}		0.594	0.6	0.606	V
Top FET RON	$R_{DS(ON)1}$			38		mΩ
Bottom FET RON	$R_{DS(ON)2}$			19		mΩ
Output Discharge Current	I_{DIS}			70		mA
Top FET Current Limit	$I_{LMT,HSFET}$			17		A
Bottom FET Current Limit	$I_{LMT, LSFET1}$	ILMT=Low	6.7	7.8	8.9	A
		ILMT=Floating	9.3	10.6	11.9	A
		ILMT=High	12	13.3	14.8	A
Bottom FET Reverse Current Limit	$I_{LIM,LSFET2}$		1.5	3	4.5	A
Soft-start Time	t_{SS}			1.3		ms
EN/MODE Rising Threshold	V_{ENH}		1			V
EN/MODE Falling Threshold	V_{ENL}				0.4	V
ILMT Rising Threshold	V_{ILMTH}		Vcc-0.5			V
ILMT Falling Threshold	V_{ILMTL}				0.5	V
Switching Frequency	f_{OSC}	V_{OUT}=5V	510	600	690	kHz
Min ON Time	$t_{ON,MIN}$	V_{IN}=V_{INMAX}		50		ns
Min OFF Time	$t_{OFF,MIN}$			150		ns
VCC Output Voltage	V_{CC}	With 1mA load	3.2	3.3	3.4	V
Output Over Voltage Threshold	V_{OVP}	V_{FB} rising	115	120	125	%V_{REF}
Output Over Voltage Hysteresis	$V_{OVP,HYS}$			1.5		%V_{REF}
Output OVP Delay	$t_{OVP,DLY}$			20		μs
Output Under Voltage Protection Threshold	V_{UVP}	V_{FB} falling	57.5	62.5	67.5	%V_{REF}
Output UVP Delay	$t_{UVP,DLY}$			200		us
Power Good Threshold	V_{PG}	V_{FB} rising (Good)		92		%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$			1.5		%V_{REF}
Power Good Delay	$t_{PG,RISING}$	Low to high		200		μs
	$t_{PG,FALLING}$	High to low		10		μs
Bypass Switch Turn-on Voltage	V_{BYP}		2.97	3.1	3.21	V
Bypass Switch Switchover Hysteresis	$V_{BYP,HYS}$			0.15		V
Bypass Switch OVP	$V_{BYP,OVP}$			120		%V_{CC}
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown hysteresis	T_{HYS}			15		℃

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

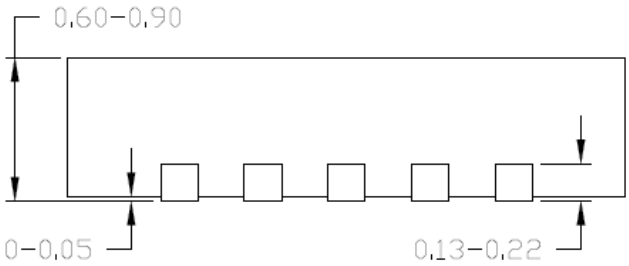
Note 2: Package thermal resistance is measured in the natural convection at T_A = 25°C on a four-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

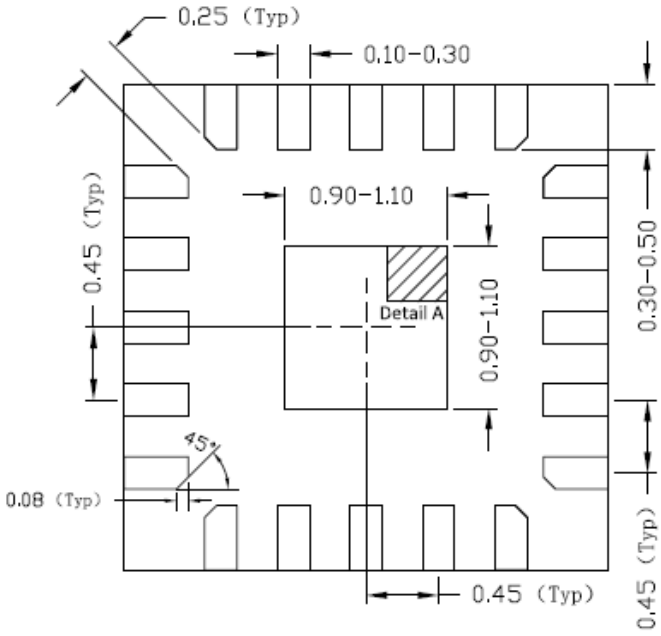
QFN3×3-20 Package Outline

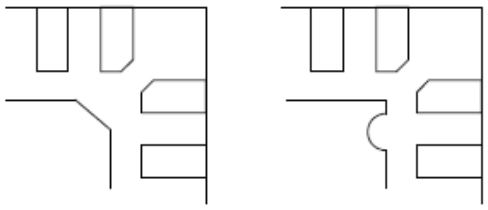


Top view



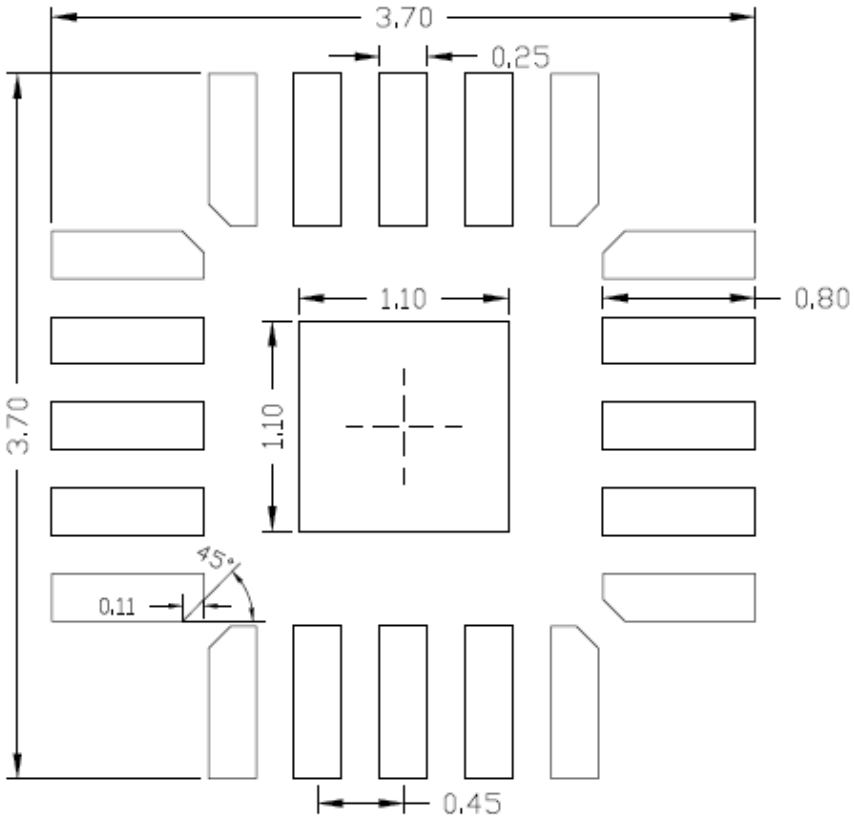
Side view





Detail A
Pin1 Identifier: two options

Bottom view

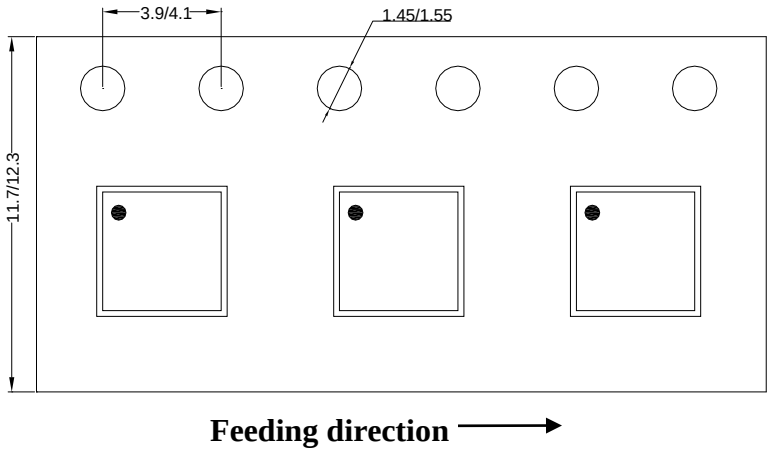


Recommended PCB layout
(Reference only)

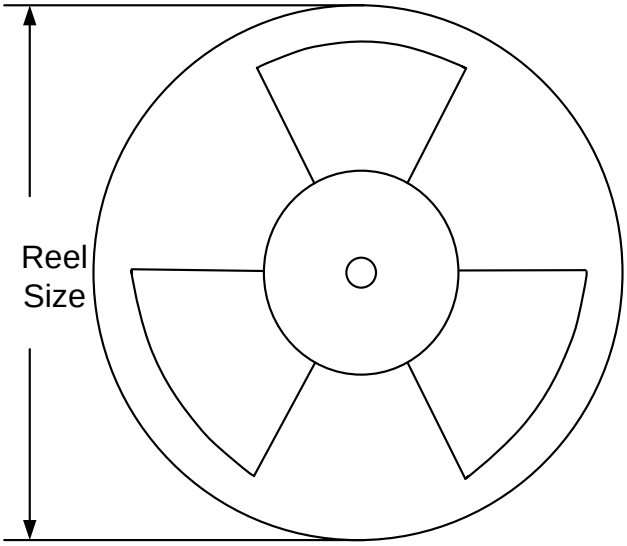
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

Taping & Reel Specification

1. QFN3×3-20 taping orientation



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3×3	12	8	13"	400	400	5000

3. Others: NA